PAT9125EL: Miniature Optical Navigation Chip

General Description

The PAT9125EL is PixArt Imaging's miniature low power optical navigation chip using PixArt's LASER-based optical navigation technology enabling digital surface tracking. It integrates an optical chip and a LASER light source in a single miniature package, providing wide depth of field (DOF) range on glossy surfaces, and design flexibility into highly space constraint devices. This tracking system also does not require code wheel, code strip and any special marking on tracking surface for motion control or tracking purposes. It is recommended for use in hermetic or enclosed mechanical system design and applications. LASER power calibration process is NOT required in the complete system; it was pre-calibrated at chip level which helps to facilitate high volume assembly.

Key Features

- Miniature reflowable SMT package with built-in VCSEL LASER light source in a single package
- Wide DOF range on glossy surfaces, e.g. stainless steel (STS)
- No lens is needed
- Compliance to IEC/EN 60825-1 Eye Safety
  - Class 1 LASER power output level
  - On-chip LASER fault detection circuitry
- Support I^{2}C or 3-wire SPI or interface
- Programmable resolution up to 1,275cpi (on flat STS)
- Motion detection interrupt output
- Efficient low power management with programmable sleep modes & downshift time
- Internal oscillator – no external clock input needed

Applications

- Suitable for space-constraint and battery-powered wireless devices
- Devices that requires tracking on surfaces with wide DOF working range
- Devices that require tracking on small diameter of shaft and suitable for wearable and portable devices

Key Parameters

Parameter	Value
Supply Voltage	VDD : 2 connection types type1 2.1 ~ 3.3V type2 1.7 ~ 1.9V
	VLD : 2.7 ~ 3.3V
Control Interface	I^{2}C or 3-wire SPI
Distance to tracking surface (DOF)	1 ~ 30mm (on STS surface)
Max. tracking speed	On flat STS ▪ 30 ips @ distance ≧ 3mm ▪ 10 ips @ distance 1~3mm On 1.0mm diameter STS shaft ▪ 900 rpm @ distance ≧ 3mm ▪ 300 rpm @ distance 1~3mm
Max Resolution	~1,275 cpi (on flat STS) or ~630 counts/rev (on 1.0mm diameter STS shaft at 1.0mm distance)
Operating current (Average @ VDD = VLD = 3.3V)	Run : 0.7mA Sleep1/2 : 25µA / 10uA Power down : 5µA
Light Source	VCSEL LASER 850 nm
Package Size LWH	3.5 x 3.2 x 1.0 mm

Ordering Information

Part Number	Interface	Package Type
PAT9125EL-TKIT	I^{2}C	LGA 8-pin
PAT9125EL-TKMT	SPI	LGA 8-pin

Lead (Pb) Free
RoHS 6 fully compliant

For any additional inquiries, please contact us at http://www.pixart.com/contact.asp

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1.0 Introduction

1.1 Overview

PAT9125EL is a high performance and an ultralow power CMOS-processed optical navigation chip with the integrated digital image process algorithm/circuits and a VCSEL LASER as the light source. It is based on PixArt's optical navigation technology of LASER which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the speed, the direction and the magnitude of motion. The displacement X and Y information are available in registers. A host controller can read and translate the displacement X and Y information from the SPI or I^2C serial interface.
Note: Throughout this document PAT9125EL is referred to as the chip.

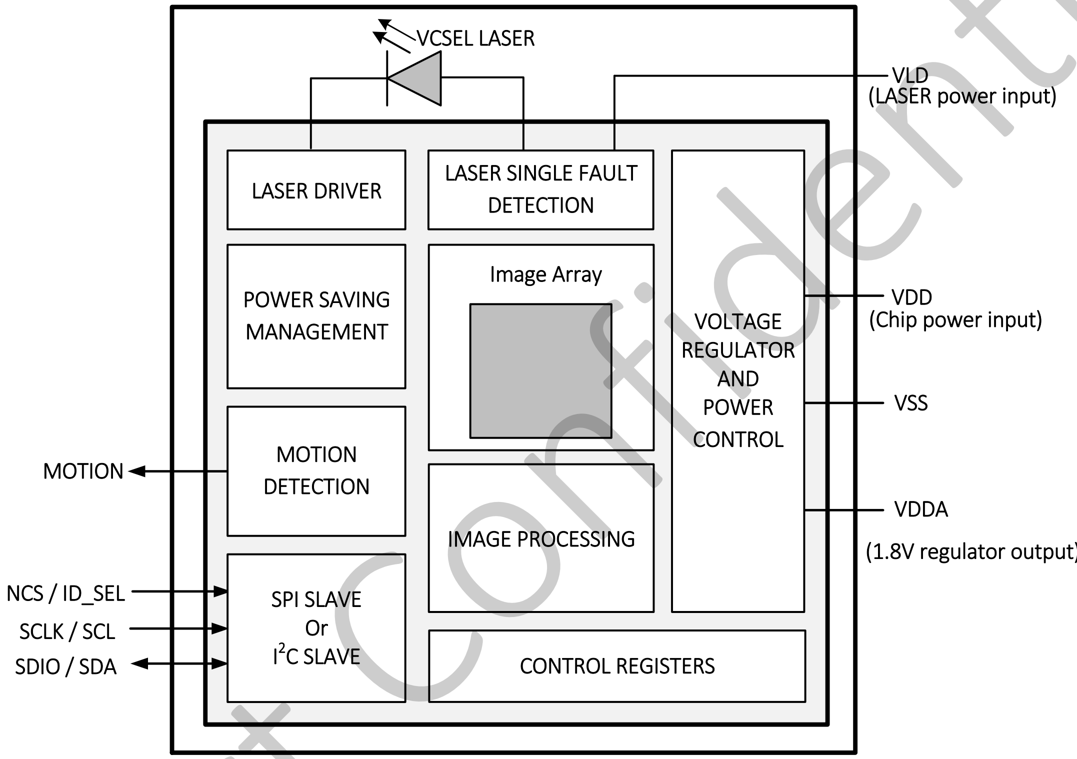


Figure 1. Functional Block Diagram

1.2 Signal Description

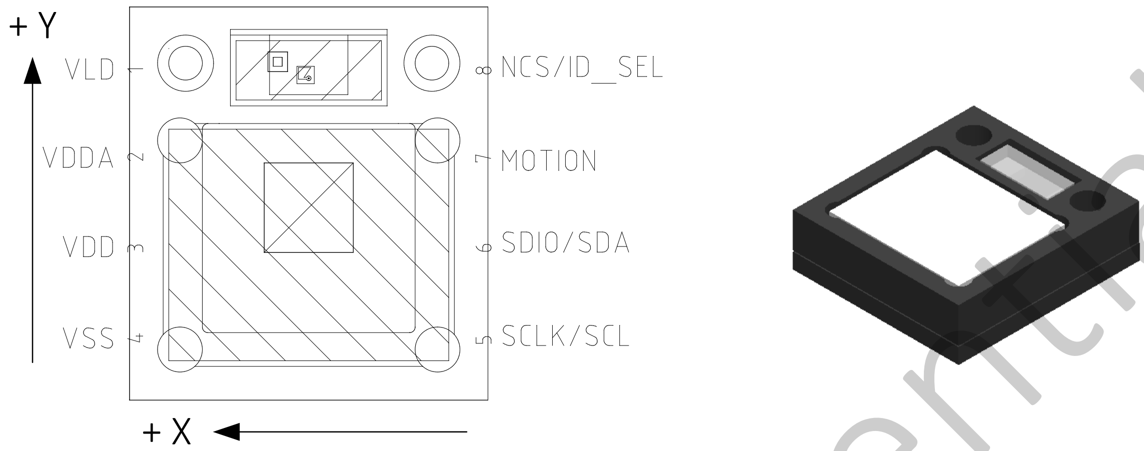


Figure 2. Pin Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name		Type	Description
	SPI	I²C		
1	VLD	VLD	PWR	Anode of the VCSEL LASER, voltage range: 2.7V ~ 3.3V
2	VDDA	VDDA	PWR	VDD is the main power supply for IC circuits High voltage Segment (VDD: 2.1V ~ 3.6V): VDDA is 1.8V regulator output and should connect a 4.7uF capacitor to ground Low Voltage Segment (VDD: 1.7V ~ 2.1V): VDDA should connect to VDD directly
3	VDD	VDD	PWR	
4	VSS	VSS	GND	Chip ground
5	SCLK	SCL	IN	SCLK : Clock input for SPI interface SCL : Clock input for I²C interface
6	SDIO	SDA	I/O	SDIO : Bi-directional I/O for SPI interface SDA : Bi-directional I/O for I²C interface
7	MOTION	MOTION	OUT	Motion detection output (active low)
8	NCS	ID_SEL	IN	NCS : Chip select for 3-wire SPI interface (active low) ID_SEL : Slave ID (7-bit) Selection for I²C interface High = 0x73, Low=0x75, NC = 0x79
9	TEST	TEST	NC	This pin is located on the back of the chip and is for PixArt testing purpose. Please do NOT connect it to any part of the PCB. Please refer to Figure 9.

1.3 Potential Tracking Mechanisms

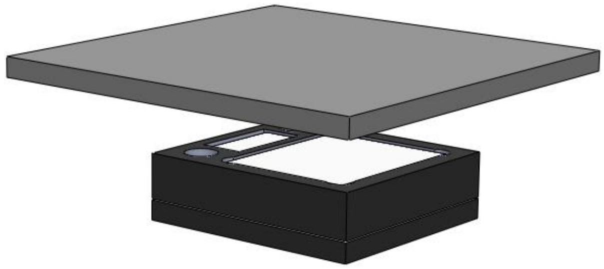


Figure 3. Tracking on a Moving Surface

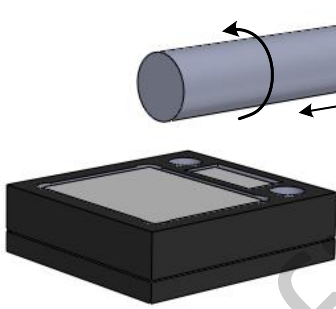


Figure 4. Tracking on the Side of a Rotational Shaft

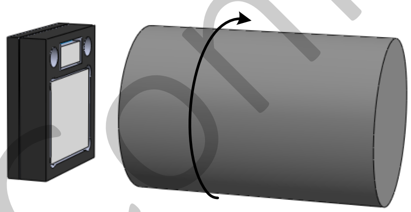


Figure 5. Tracking on the end of a Rotational Shaft

Figure 6. Tracking on a Disk Edge

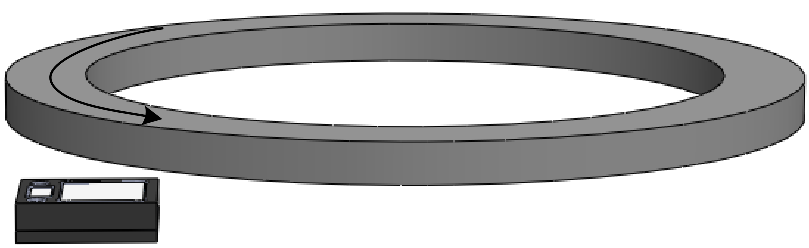


Figure 7. Tracking on a Rotational Bezel

1.4 Terminologies

Term	Description
ACK	Acknowledge bit of I^2C bus
CPI	Counts per Inch
DOF	Depth of Field
FPS	Frames per Second
I^2C	Inter-Integrated Circuit
IPS	Inches per Second
LD	LASER Diode
LGA	Land Grid Array
LOP	LASER output power, unit: uW (micro-watt)
NA	Not-acknowledge bit of I^2C bus
RPM	Revolutions per Minute
SPI	Serial Peripheral Interface
STS	Stainless Steel
VCSEL	Vertical-Cavity Surface-Emitting LASER

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	T_{STG}	-40	85	°C	
Power Supply Voltage	V_{DC}	-0.3	3.9	V	
Signal Input Voltage	V_{IN}	-0.3	V_{DC}	V	For all input I/O
Lead Solder Temp	T_{SOL}	-	260	°C	Non-condensing, Non-biased
ESD	V_{HBM}	-	2	kV	All pins, Human Body Model MIL 883 Method 3015

Notes:

1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
4. Functional operation should be restricted to the Recommended Operating Conditions.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_A	-20	-	60	°C	
Power Supply Voltage	VDD	2.1	-	3.3	V	For chip operated in High Voltage Segment
		1.7	1.8	1.9	V	For chip operated in Low Voltage Segment
	VLD	2.7	3.0	3.3	V	For LASER Power
Supply Noise	V_{NPP}	-	-	100	mV	Peak to peak voltage within 10kHz – 80 MHz
Distance to Tracking Surface (DOF)	Z	1		30	mm	On STS surface (refer to Notes below)
Tracking Speed	V_{SP}	-	-	30	ips	Based on flat STS with distance ≧ 3mm
				10	ips	Based on flat STS with distance 1~3mm
				900	rpm	Based on 1.0mm diameter STS shaft with distance ≧ 3mm
				300	rpm	Based on 1.0mm diameter STS shaft with distance 1~3mm

Notes:

1. PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.
2. When the distance to tracking surface is < 3mm, the reported CPI resolution could be lower than the CPI value at ≧ 3mm. Please refer to Figure 8 below.

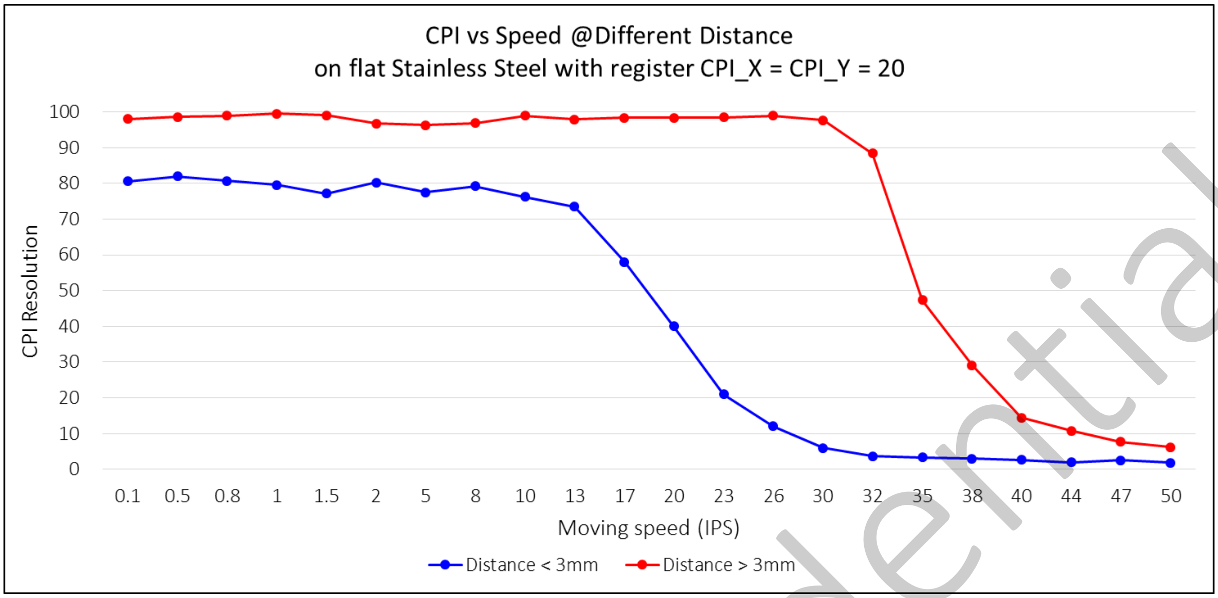


Figure 8. CPI vs Speed @Different Distance

2.3 DC Characteristics

Table 4. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Run mode current	I_{RUN}	-	0.7	-	mA	Tracking speed dependent @VDD=VLD=3.3V on STS
Sleep 1 mode current	I_{SLP1}	-	25	-	µA	Based on 32ms sampling period @VDD=VLD=3.3V on STS
Sleep 2 mode current	I_{SLP2}	-	10		µA	Based on 128ms sampling period @VDD=VLD=3.3V on STS
Power Down current	I_{PD}	-	5	10	µA	@VDD=VLD=3.3V
Input Voltage High	V_{IH}	VDD*0.7	-	-	V	For NCS, SCLK, SDIO, MOTION pins
Input Voltage Low	V_{IL}	-	-	VDD*0.3	V	
Output Voltage High	V_{OH}	VDD-0.4	-	-	V	
Output Voltage Low	V_{OL}	-	-	0.4	V	

Notes: All the parameters are tested under operating conditions: T_A = 25°C

3.0 Mechanical Specifications

3.1 Mechanical Dimension

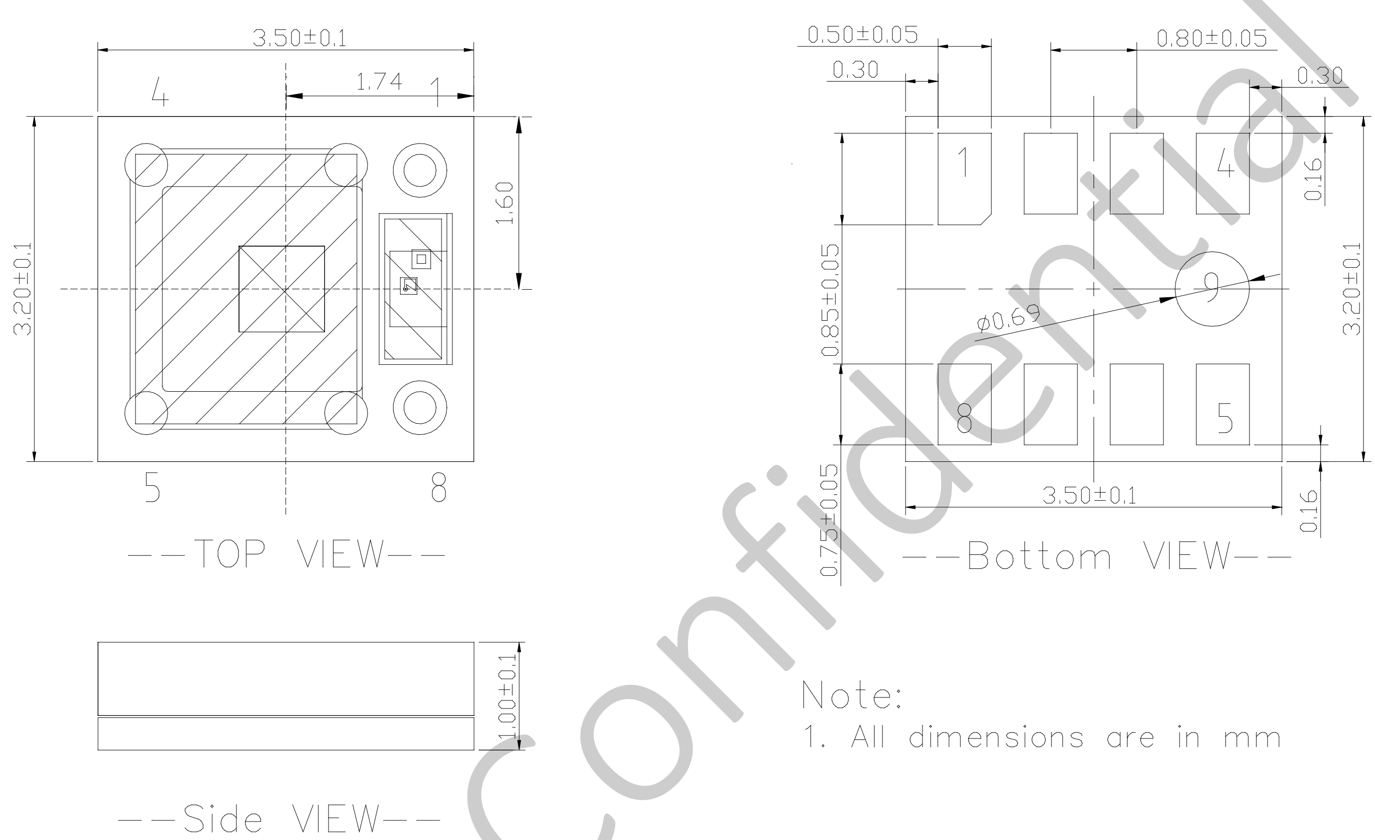


Figure 9. Package Outline Diagram

4.0 Power-up Sequence Requirements

If the VDD and VLD for the chip are not sourced from the same power supplies input, a power-up sequence is applicable on these two power inputs to avoid excessive current leakage or occurrence of unexpected system instability happening on the chip.

1. VDD must be powered up first or at the same time with VLD. VLD can never be powered up earlier than VDD.
2. VDD must always be applied with power supply when VLD is powered.
3. It is recommended to activate the I^2C or SPI control 10ms after a stable VDD power supply is applied to the chip.

Failure in following the requirements above may have induced risk on high current leakage on the VLD that may damage the LASER diode integrated in the package.

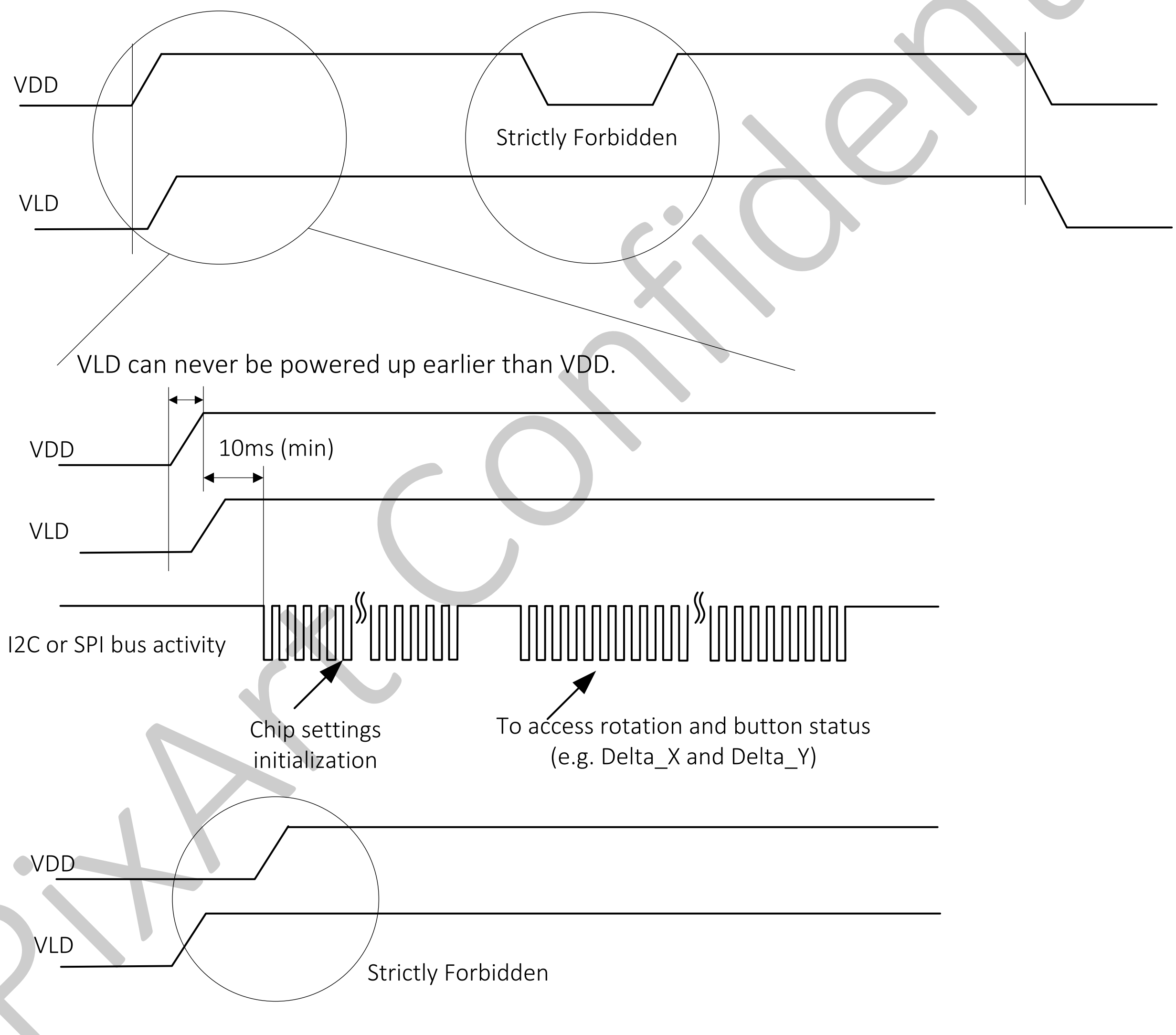


Figure 10. Power-up Sequence Requirements

5.0 Power Supply Configuration

The chip has 2 segments for power supply configuration, the High Voltage Segment and the Low Voltage Segment. With these two segments, the chip provides the flexibility to applications with different power consideration. For High Voltage Segment, which means the power supply voltage ranges from 2.1V to 3.6V, the power pins VDD and VDDA of the chip should be connected as shown in Figure 11. For Low Voltage Segment, which means the power supply voltage ranges from 1.7V to 2.1V, the power pins VDD and VDDA of the chip should be connected as shown in Figure 12.

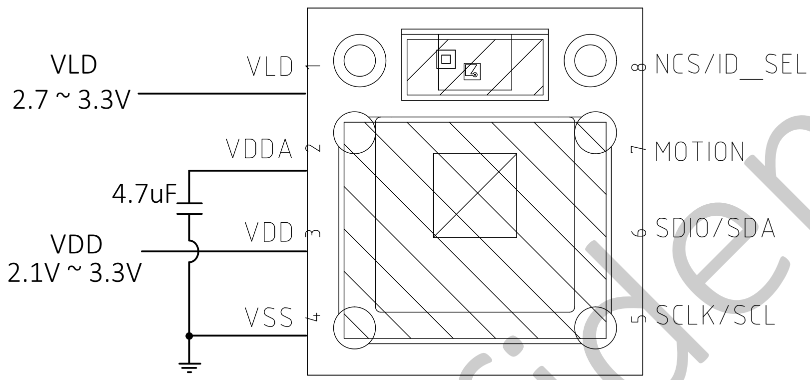


Figure 11. High Voltage Segment

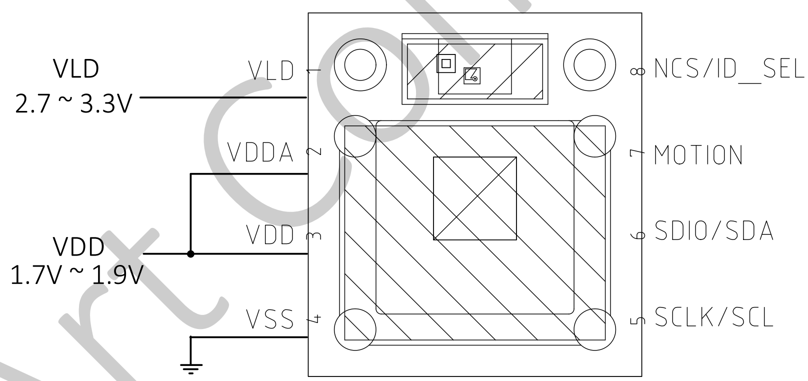


Figure 12. Low Voltage Segment

The chip's power-up default settings are for the High Voltage Segment. If users want to use the Low Voltage Segment, register address 0x4B should be set value 0x04 after the power-up sequence. If this register is not set properly, the chip would consume extra power due to the current leakage of the internal regulator.

Write address 0x7F = 0x00;	*to switch to register bank0*
Write address 0x09 = 0x5A;	*to disable Write Protect*
Write address 0x4B = 0x04;	*to turn off internal regulator for Low Voltage Segment*
Write address 0x09 = 0x00;	*to enable Write Protect*

6.0 Reference Schematics

6.1 Schematics for I²C Interface (PAT9125EL-TKIT)

The chip supports standard I²C interface and the SCL clock speed is up to 1MHz. Three different Slave IDs can be selected from the ID_SEL pin (High = 0x73, Low=0x75, NC = 0x79). Notice that 5KΩ of R1 and R2 (SCL/SDA bus pull-high resistors) is just for reference and the resistance might have to be adjusted according to the overall I²C bus loading of user's whole system.

6.1.1 High Voltage Segment (VDD : 2.1V ~ 3.3V)

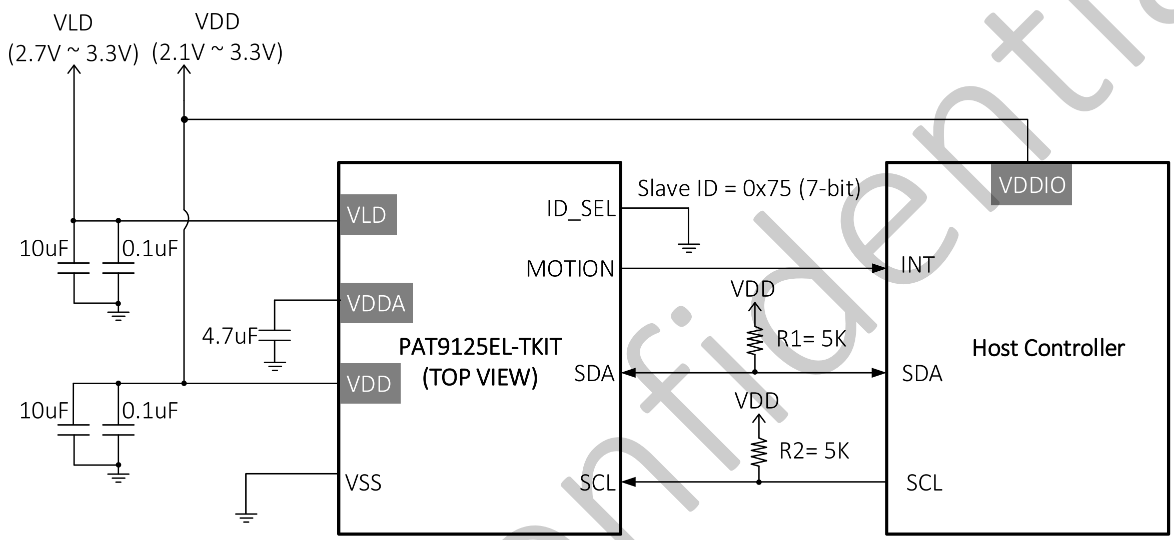


Figure 13. Schematics for High Voltage Segment (I²C Interface)

6.1.2 Low Voltage Segment (VDD : 1.7V ~ 1.9V)

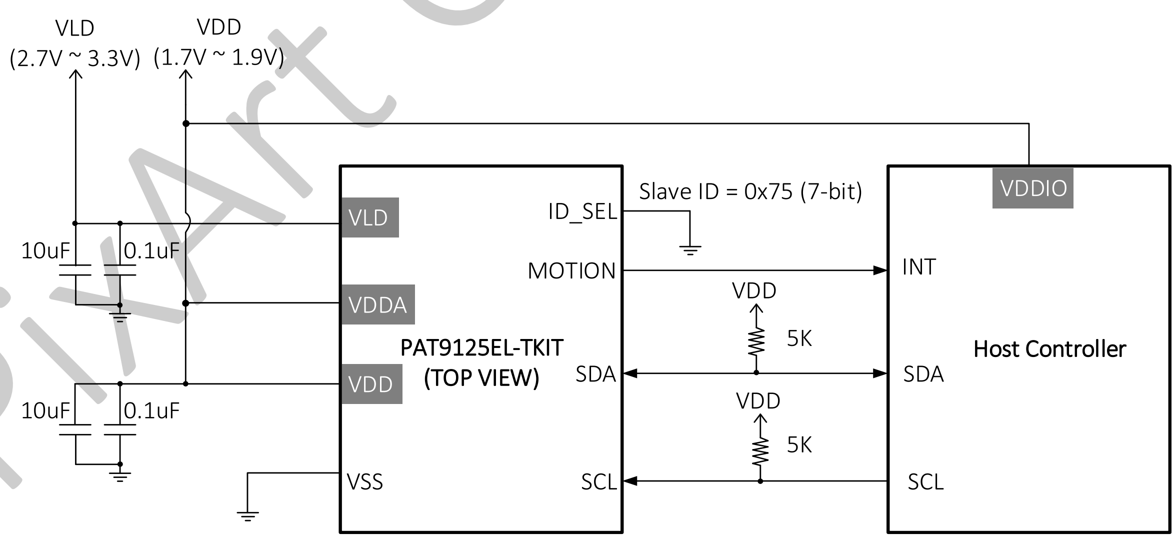


Figure 14. Schematics for Low Voltage Segment (I²C Interface)

6.2 Schematics for SPI Interface (PAT9125EL-TKMT)

The chip only supports simplified 3-wire SPI slave mode, while some host controllers only support standard 4-wire SPI master mode. In this case, users can connect the host controller to the chip using the method shown below to communicate each other. Notice that 3.3KΩ for R1 is just for reference and the resistance might have to be modified according to different I/O capability of different host controllers.

6.2.1 High Voltage Segment (VDD : 2.1V ~ 3.3V)

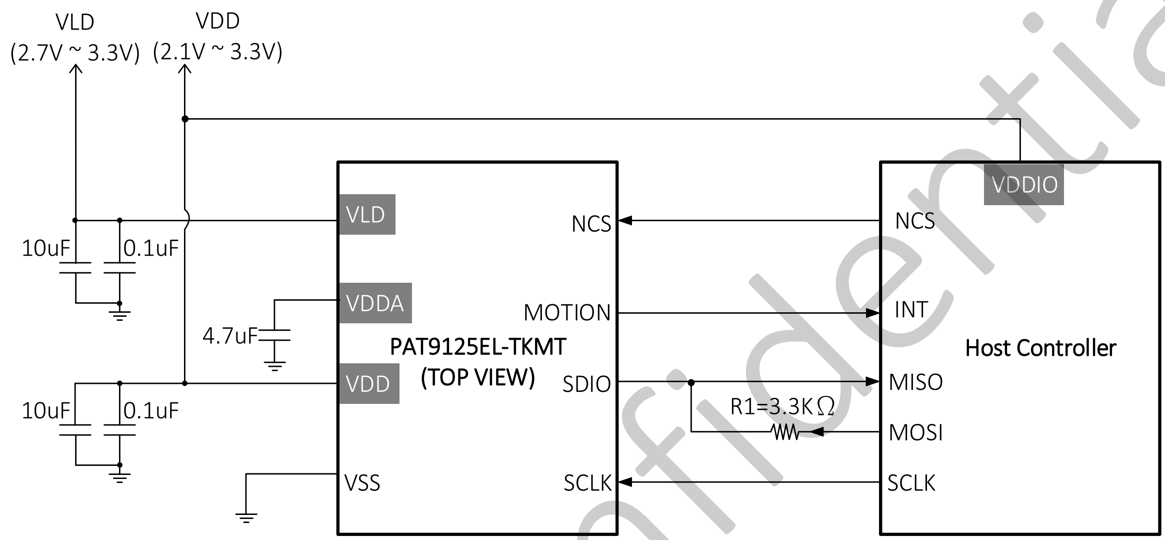


Figure 15. Schematics for High Voltage Segment (SPI Interface)

6.2.2 Low Voltage Segment (VDD : 1.7V ~ 1.9V)

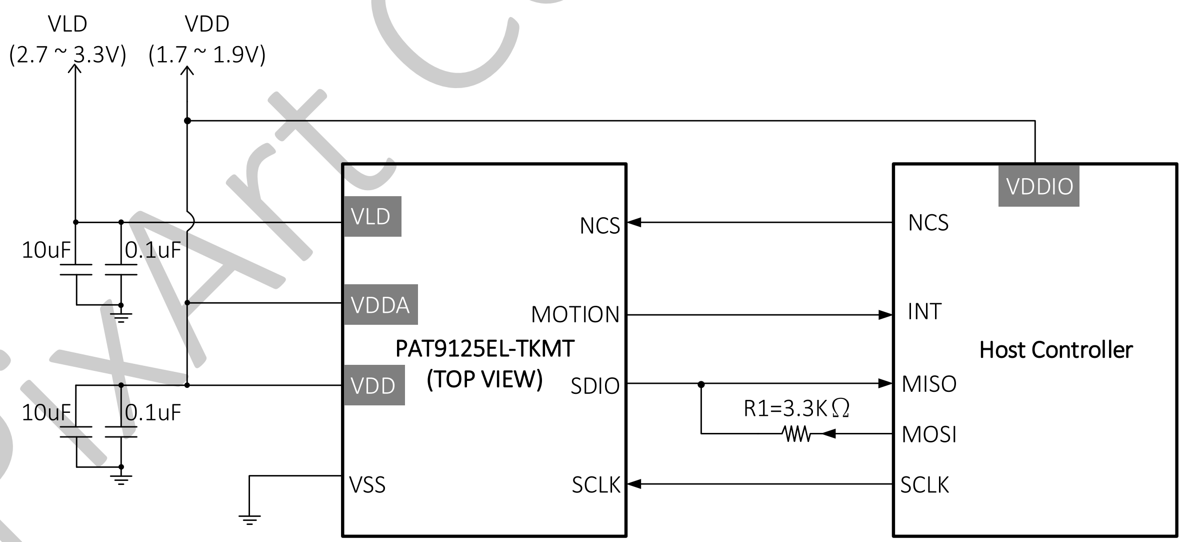


Figure 16. Schematics for Low Voltage Segment (SPI Interface)

7.0 I²C Serial Interface for PAT9125EL-TKIT

7.1 Signal Description

The chip is implemented as a slave-only device, so it never drives SCL, and only drives SDA during read cycles and transfer acknowledge bits.

- SCL: The SCL signal is always driven by the master. SCL synchronizes the serial transmission of data bits on SDA. The frequency of SCL may vary throughout a transfer, as long as it meets all timing requirements.
- SDA: The SDA signal is for the host to read from or write to the chip. The host drives SDA under three conditions (1) when sending the Slave ID and address to the chip (2) when writing data to the chip (3) when responding with an ACK or NAC to the chip after receiving data from the chip. The chip drives the SDA under two conditions (1) when responding with an Acknowledge (ACK) bit after receiving data from the host (2) when sending data to the host at the host's request. Data is sent in eight-bit packets.

7.2 Slave ID Selection

The chip uses 7-bit addressing and the slave ID is decided by the status of ID_SEL input pin (High = 0x73, Low=0x75, NC = 0x79).

7.3 Start and Stop of Synchronous Operation

All communications take 9 clocks to complete, 8 for the data and the 9th bit is for acknowledge. Transfers are initiated with an S condition and terminated with the P condition. During the 8 bits of data transmissions, SDA may change while clock is low. SDA changes while clock is high in an S or P condition.

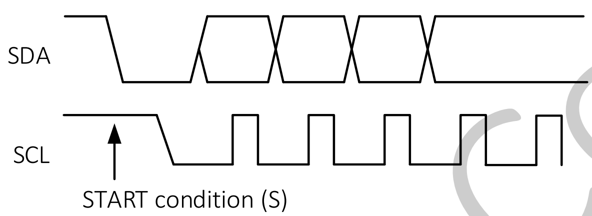


Figure 17. START Conditions

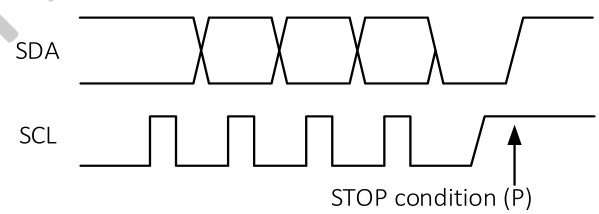


Figure 19. STOP Conditions

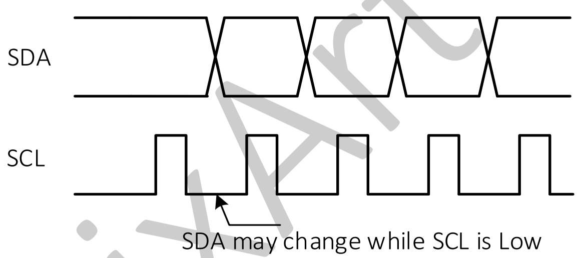


Figure 18. Data May Change When SCL is Low

Bytes that are transferred from the master to the slave are acknowledged by the slave. The slave acknowledges by driving a 0 on SDA during the 9th clock. This includes write data and slave address packets. When a byte is transferred from the slave to the master (read data), the slave ignores the SDA pin during the 9th clock.

When packets are sent over the I²C interface, they are generally of the format. The R/W bit defines the direction of all data bytes after the S condition (Read: 1, Write: 0). In other words, it is not possible to initiate a write operation, and then switch to a read operation without completing the write.

S, <slave address, R/W>, A, data, A, data, A, ... , P

After a start condition, a single acknowledge/not-acknowledge bit follows each eight-bit data packet. The device receiving the data drives the acknowledge/not-acknowledge signal on SDA. Acknowledge (ACK) is defined as 0 and not-acknowledge (NA) is defined as 1.

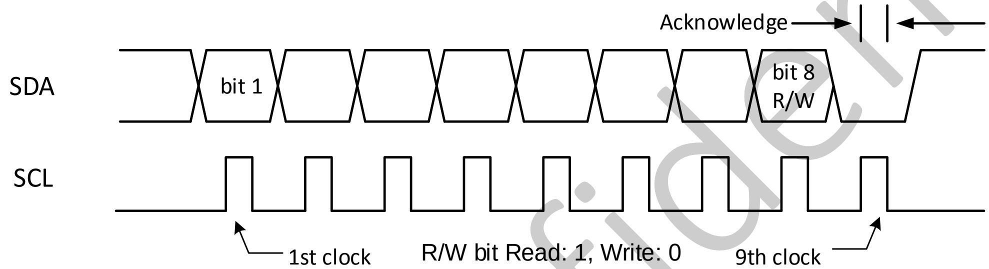


Figure 20. Acknowledge Bit

7.4 Driven Packets

For a host driven packet, the host initiates all data transmission with a START condition. Next, slave address and register address packets are sent. If there is a device address match, the chip then responds to each Eight-bit data transmission with an acknowledge signal (SDA = 0). Data is transmitted with the most significant bit first. To terminate the transfer of host driven packets, the host follows the chip's ACK with a STOP condition. The host can also issue a START condition after the chip's ACK, if it wants to start a new data transfer.

S	SlaveID(7bit)	W(0)	A	0	Addr(7bit)	A	Data(8bit)	A	P
	MSB	LSB		MSB	LSB		MSB LSB		

Figure 21. I²C Host Driven Packet (Write)

For a chip driven packet, by request of the host, the chip acknowledges a read request, and then outputs a data byte transmitting the most significant bit (7) first. If the host intends to continue the data transfer, the host acknowledges the chip. If the host intends to terminate the transfer, it responds with not-acknowledge (NA, SDA = 1), and then drives SDA to generate a STOP condition. The host can also drive a START condition, if it wants to begin a new data transfer with the same chip.

S	SlaveID(7bit)	W(0)	A	0	Addr(7bit)	A	P	S	SlaveID(7bit)	R(1)	A	Data(8bit)	NA	P
	MSB	LSB		MSB	LSB				MSB	LSB		MSB LSB		

Figure 22. I²C Slave Driven Packet (Read)

Two types of the Burst Read are provided. Since the valid address of the chip is only 7-bit, the MSB of the address field in the driven packet can be used to decide which type is selected. When the MSB of the address field is 0, the data of consecutive address can be read out in sequence. While if the MSB of the address field is 1, the data of the address which is specified in the address field (7-bit) can be read out repeatedly.

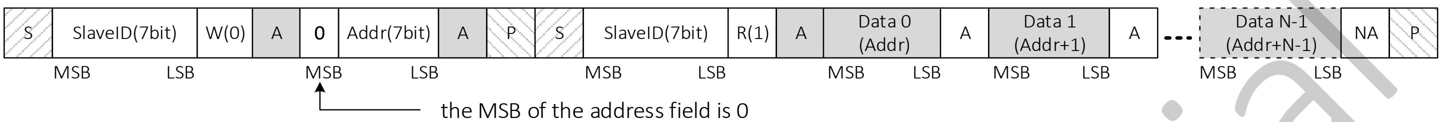


Figure 23. I²C Slave Driven Packet (Burst Read of consecutive addresses)

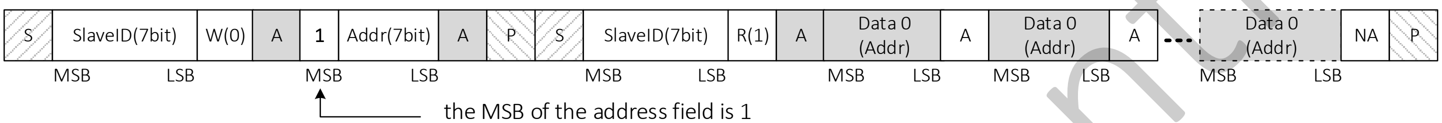


Figure 24. I²C Slave Driven Packet (Burst Read of single address)

7.5 I²C Timing

Table 5. I²C Timing Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCL clock frequency.	F_{scl}	-	-	400	kHz	
Hold time for Start/Repeat Start. After this period, the first clock pulse is generated.	$t_{HD.STA}$	0.6	-	-	µs	
Set-up time for a repeated Start.	$t_{SU.STA}$	0.6	-	-	µs	
Low period of SCL clock.	t_{LOW}	1.3	-	-	µs	
High period of SCL clock.	t_{HIGH}	0.6	-	-	µs	
Data hold time.	$t_{HD.DAT}$	0	-	-	µs	
Data setup time.	$t_{SU.DAT}$	250	-	-	ns	
Rise time of both SDA and SCL signals.	t_r	-	-	300	ns	
Fall time of both SDA and SCL signals.	t_f	-	-	300	ns	
Set-up time for STOP condition.	$t_{SU.STO}$	0.6	-	-	µs	
Bus free time between a STOP and START.	t_{BUF}	1.3	-	-	µs	

Notes: Maximum current is 5mA and capacitance load spec. =100pF

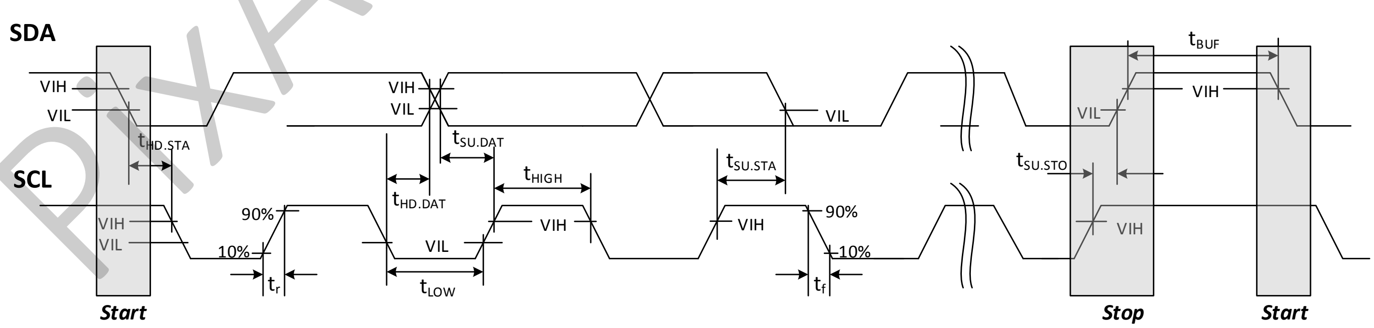


Figure 25. I²C Timing Diagram

8.0 3-Wire SPI Serial Interface for PAT9125EL-TKMT

The chip supports 3-wire Serial Peripheral Interface (SPI). The host controller can use the SPI to write and read registers in the chip, and to read out the motion information. The host controller always initiates communication; the chip never initiates data transfers. NCS, SCLK and SDIO may be driven directly by the host controller. SDIO may also be driven by the chip when data is read out from chip registers.

- NCS: Chip select input (active low). NCS needs to be low to activate the SPI; otherwise, SDIO will be at high-Z state and SCLK will be ignored. NCS can also be used to reset the SPI in case a communicational error happens.
- SCLK: Clock input. It is always generated by the host controller.
- SDIO: Bi-directional input/output data

Note : The chip only supports SPI mode 3 (that is, CPOL=1 and CPHA=1). Please make sure the SPI master in the host controller is configured as mode 3.

8.1 Transmission Protocol

The transmission protocol is a 3-wire link, half duplex protocol between the host controller and the chip. All data changes on SDIO are initiated by the falling edge on SCLK. The host controller always initiates communication; the chip never initiates data transfers. The transmission protocol consists of the following two operation modes.

- Write Operation
- Read Operation

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has a bit-7 as its MSB to indicate data direction. The second byte contains the data.

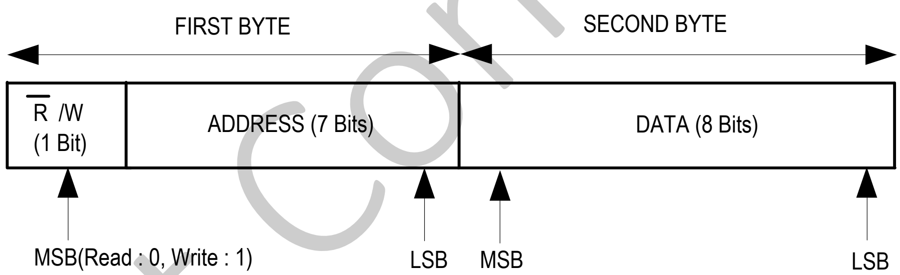


Figure 26. Transmission Protocol

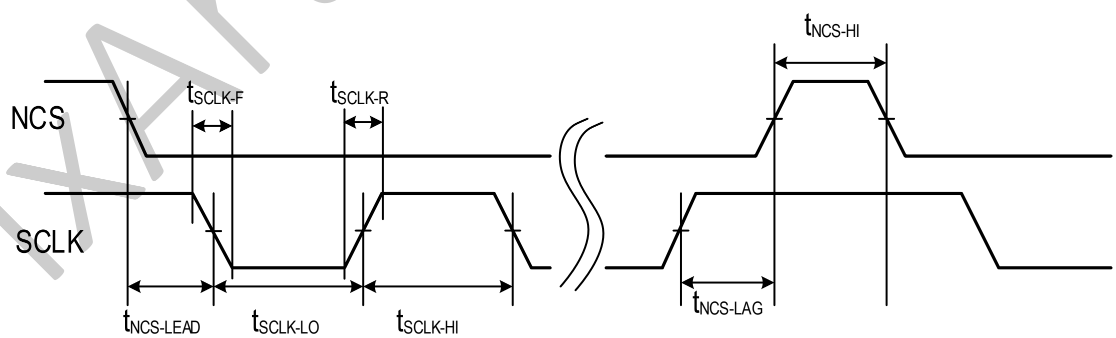


Figure 27. NCS vs SCLK Timing Requirement

8.1.1 Write Operation

A write operation, defined as data is going from the host controller to the chip, is always initiated by the host controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The communication is synchronized by SCLK. The host controller changes SDIO on the falling edges of SCLK and the chip reads SDIO on the rising edges of SCLK.

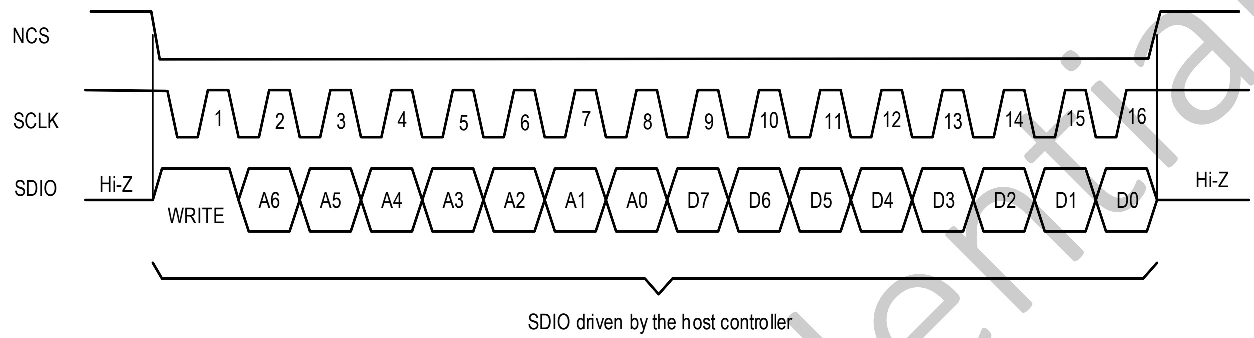


Figure 28. Write Operation

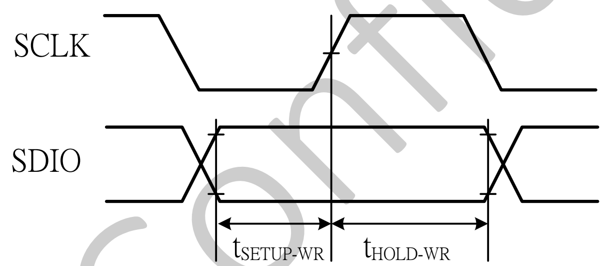


Figure 29. SDIO setup and hold time during write operation

8.1.2 Read Operation

A read operation is initiated by the host controller and consists of two bytes. The first byte contains the address specified by the host controller and has a "0" as its MSB to indicate data direction. The second byte contains the data which is outputted by the chip. The communication is synchronized by SCLK. SDIO is changed on the falling edges of SCLK and is read on every rising edge of SCLK. The host controller must release SDIO bus and handover the control of SDIO bus to the chip on the falling edge of last address bit. Do take note that the delay time ($t_{PREP\text{-}RD}$) between the rising edge of the 8^{th} SCLK and the falling edge of 8^{th} SCLK should be no less than 10us to ensure the chip has enough time to prepare data for reading.

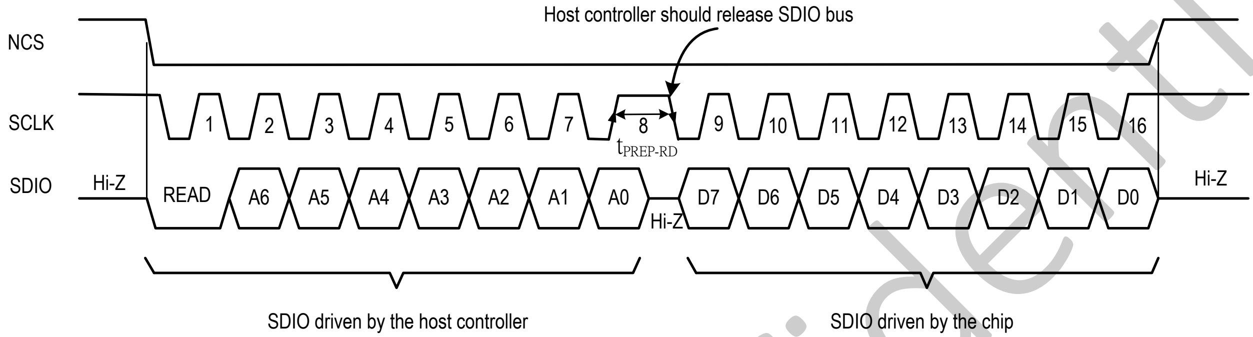


Figure 30. Read Operation

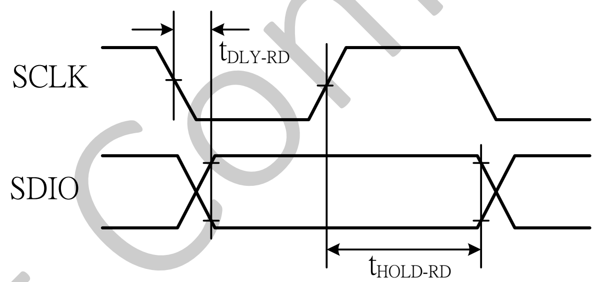


Figure 31. SDIO delay and hold time during read operation

8.2 SPI Timing

Table 6. SPI Timing Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
SCLK frequency	F_{SCLK}	-	-	2	MHz	SPI max. operation frequency
SCLK High Time	$t_{SCLK-HI}$	250	-	-	ns	SCLK min. high time
SCLK Low Time	$t_{SCLK-LO}$	250	-	-	ns	SCLK min. low time
SCLK Rise Time	t_{SCLK-R}	-	-	30	ns	SCLK max. rise time
SCLK Fall Time	t_{SCLK-F}	-	-	30	ns	SCLK max. fall time
NCS Enable Lead Time	$t_{NCS-LEAD}$	1	-	-	µs	From NCS falling to first SCLK falling
NCS Enable Lag Time	$t_{NCS-LAG}$	1	-	-	us	From Last SCLK rising to NCS rising
NCS min. High Time	t_{NCS-HI}	2	-	-	us	From previous NCS rising to next NCS falling
SDIO Write Setup Time	$t_{SETUP-WR}$	250	-	-	ns	SDIO data valid before SCLK rising
SDIO Write Hold Time	$t_{HOLD-WR}$	250	-	-	ns	SDIO data valid after SCLK rising
SDIO delay after SCLK	t_{DLY-RD}	-	-	50	ns	From SCLK falling to SDIO data valid, no load conditions
SCLK delay for Data Preparation	$t_{PREP-RD}$	250	-	-	ns	The min. time between the rising of 8th SCLK and the falling of 8th SCLK
SDIO Read Hold Time	$t_{HOLD-RD}$	250	-	-	ns	SDIO data valid after SCLK rising
SDIO Rise Time	t_{SDIO-R}	-	30	-	ns	@C_L = 30 pF
SDIO Fall Time	t_{SDIO-F}	-	30	-	ns	@C_L = 30 pF

Note: All the parameters are tested under operating conditions: V_{DD} = 3.3V and T_A = 25°C

9.0 Methods to Read the Motion Data

Whenever the chip detects the occurrence of motion, the detected motion data (X-movement and Y-movement) is accumulated and stored in chip's internal buffer. The host controller can read out this motion data through register Delta_X_Lo, Delta_Y_Lo and Delta_XY_Hi (address 0x03, 0x04, 0x12). Before reading the motion data through these registers, be sure to read register Motion_Status (address 0x02) first to check if the MOTION bit (bit 7) is 1. If the MOTION bit is 1, the data in register Delta_X_Lo, Delta_Y_Lo and Delta_XY_Hi is valid, otherwise it is invalid.

The host controller can use the following two methods to read out the chip motion data, (1) the polling mode (2) the interrupt mode, which are described in the following two subchapters.

9.1 Read Motion Data with Polling Mode

By reading and checking register MOTION_Status (address 0x02) periodically, the host controller can get the motion data in a simple way through I^2C or SPI interface. Be noticed that the 8ms shown in the flowchart below is just for reference. The delay time might depend on the capability of the host controller and the need for different applications.

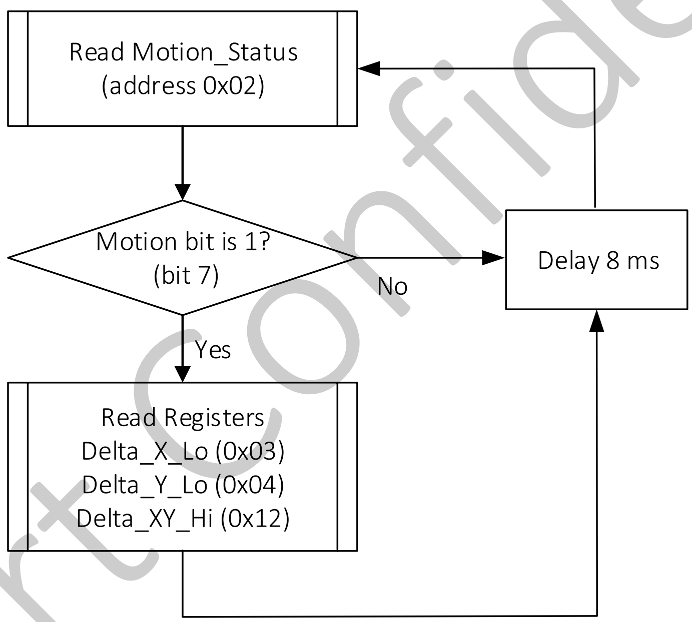
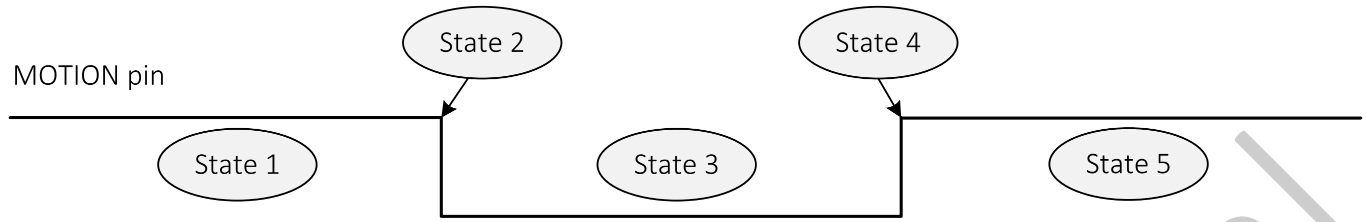


Figure 32. Read Motion Data with Polling Mode

9.2 Read Motion Data with Interrupt Mode

The MOTION pin is an indicator to show whether if any motion data is accumulated and stored in chip's internal buffer. If the MOTION pin is low, it means some motion data is still stored in the internal buffer and is waiting for the host controller to read out. If the internal buffer is cleared, the MOTION pin goes high.



State 1 : No motion detected. MOTION bit=0 and Delta_X_Lo, Delta_Y_Lo, Delta_XY_Hi are invalid. (zero values)

State 2 : Motion detected. MOTION bit=1 and Delta_X_Lo, Delta_Y_Lo, Delta_XY_Hi are valid (non-zero values).

State 3 : Motion continues. MOTION bit=1 and Delta_X_Lo, Delta_Y_Lo, Delta_XY_Hi are valid (non-zero values).

State 4 : Motion stops and the last reports of motion data stored in chip's internal buffer have been read out. MOTION bit=0 and Delta_X_Lo, Delta_Y_Lo, Delta_XY_Hi are invalid. (zero values)

State 5 : No motion detected. MOTION bit=0, Delta_X_Lo, Delta_Y_Lo, Delta_XY_Hi are invalid. (zero values)

Figure 33. Motion Pin Function

The host controller can use the MOTION pin as a level-triggered interrupt source to trigger an event of reading the motion data stored in the chip's internal buffer. Besides, when the host controller is staying at idle mode, and when the chip detects the occurrence of motion, the MOTION pin goes low. This event on MOTION pin can be used as an interrupt event to wake up the host controller. Please refer to the flowchart for below.

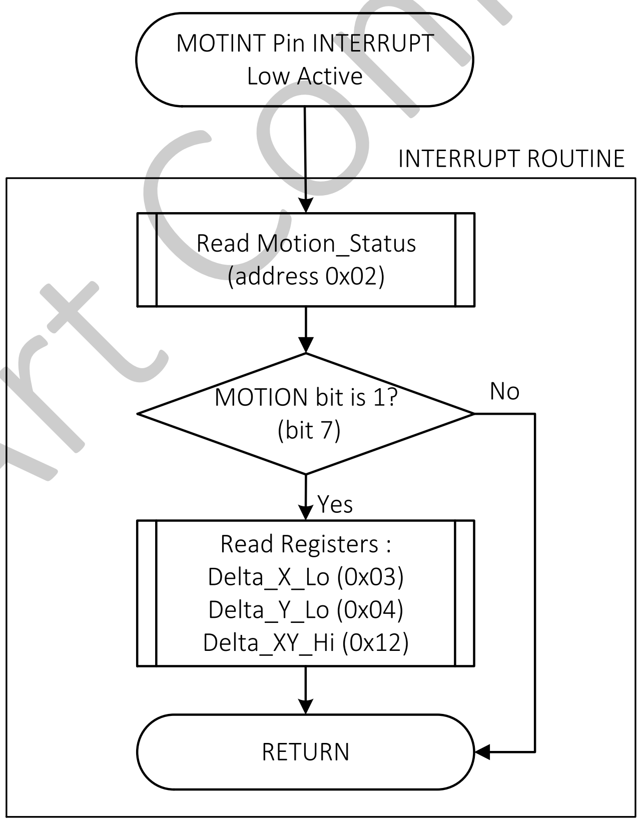


Figure 34. Read Motion Data with Interrupt Mode

10.0 Operational Modes

10.1 Power Management

The chip has two power-saving modes (Sleep1 and Sleep2). Each mode has a different motion detection period to detect the motion periodically. When left idle, the chip automatically changes from Run mode to Sleep1 mode, and finally to Sleep2 mode which consumes the least current. Be noticed that the current consumption is the lowest at Sleep2 mode and higher at Sleep1 mode, however the time required for the chip to "wake up" from Sleep2 mode to Run mode is longer than from Sleep1 mode. The entering time (Slp1_Etm, Slp2_Etm in address 0x0A and 0x0B) is the elapsed time from the time when the chip is idle to Sleep modes. The sampling frequency time (Slp1_Freq, Slp2_Freq in address 0x0A and 0x0B) is the time period to detect the motion under Sleep modes. The relationship between the entering time and the sampling frequency time is shown in figure below.

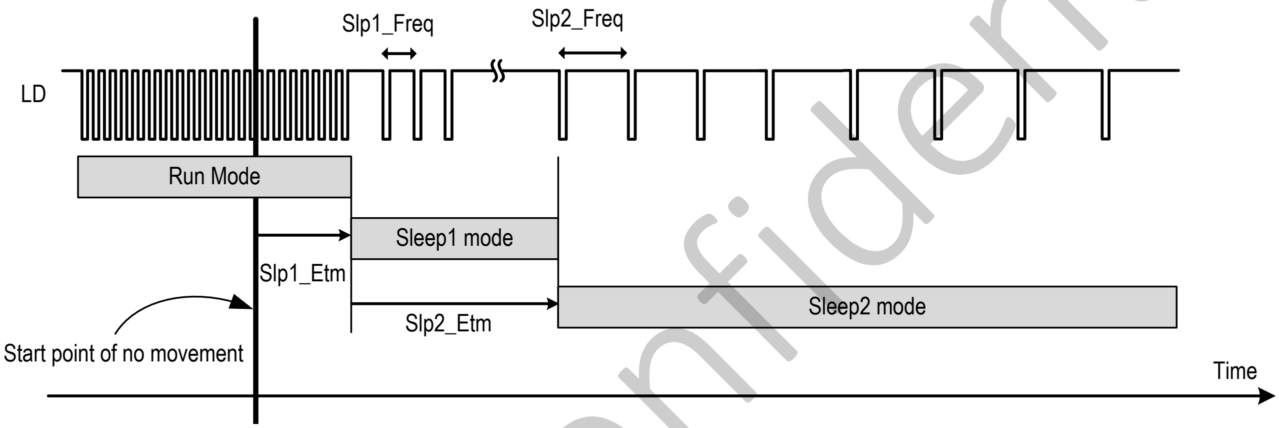


Figure 35. Power-Saving Modes

10.2 Software Power-Down

The chip can be placed in an extremely low power state (power-down mode) by setting PD_EnH bit (bit 3) in the Configuration register (address 0x06) through SPI interface. In power-down mode, all the chip register settings are retained and can be accessed through I^{2}C or SPI interface as well. To get the chip out of the power-down mode, a reset to the PD_EnH bit will do. To get more accurate motion reports, it is recommended that the host controller should wait at least 3ms before reading the motion reports after resetting the PD_EnH bit.

10.3 Software Reset

During power-up, the chip does not need an external power-on reset as there is an internal circuitry that performs power-on reset function in the chip. However the chip can also be reset by setting the RESET bit (bit 7) of Configuration register (address 0x06). Upon a software reset being executed, all the recommended register settings must be reloaded in order to keep the chip working correctly.

Be noticed that after a software reset (write value 0x97 to address 0x06) is executed on the chip, the host controller should wait at least 1ms and then write value 0x17 to the address 0x06 of the chip to ensure the chip has left the reset state.

11.0 LASER Eye Safety Protection

The chip is intended to comply with Class 1 Eye Safety Requirements of IEC 60825-1. PixArt calibrates the chip's LASER output power (LOP) to Class 1 eye safety level and store the registers values that control the LOP prior shipping out, thus no LOP calibration is required in a complete system at manufacturer site.

The chip is designed to maintain the LASER output power within Class 1 LASER Eye Safety requirements over components manufacturing tolerances under the recommended operating conditions and application circuits specified in this document. Under normal operating condition, the chip generates and regulates the drive current for the VCSEL. Increasing the LOP by other means on hardware and software can result in a violation of the Class 1 eye safety limit of 716uW.

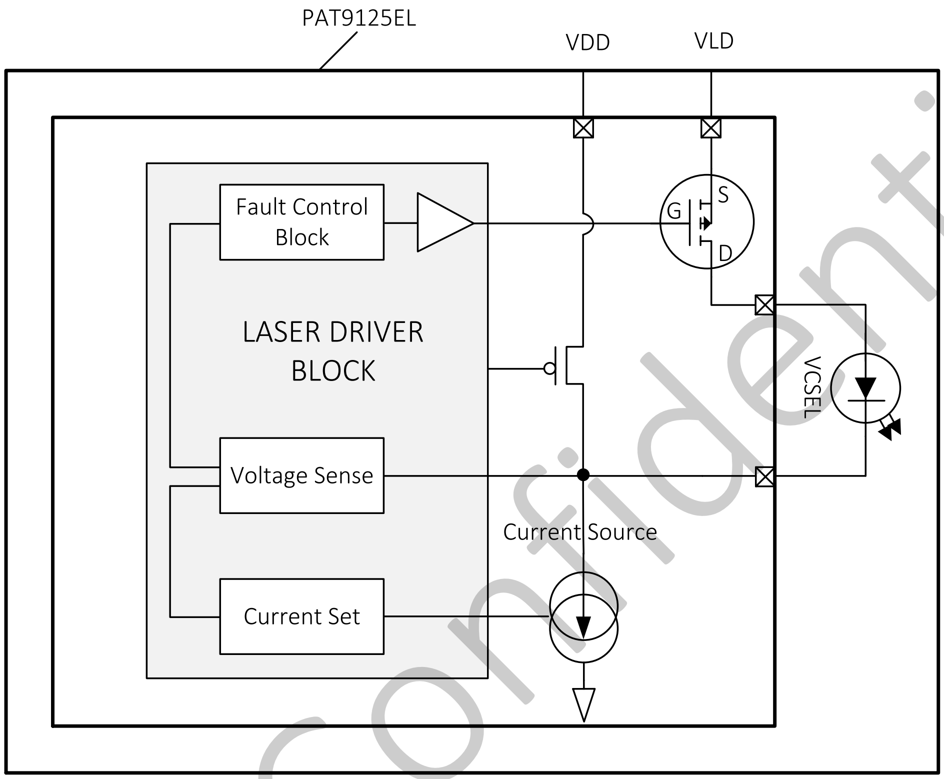


Figure 36. LASER Eye Safety Protection

12.0 Registers

12.1 Registers List

Address	Register Name	Access	Reset	Brief Description
0x00	Product_ID1	RO	0x31	Product Identifier [11:4]
0x01	Product_ID2	RO	0x91	Upper 4 bits for Product Identifier, PID [3:0] Lower 4 bits for Product Version, VID [3:0]
0x02	Motion_Status	RO	-	Motion Status information
0x03	Delta_X_Lo	RO	-	8-bit 2's complement number for X-movement data in 8-bit movement data format X-movement = Delta_X_Lo[7:0]
0x04	Delta_Y_Lo	RO	-	8-bit 2's complement number for Y-movement data in 8-bit movement data format Y-movement = Delta_Y_Lo[7:0]
0x05	Operation_Mode	R/W	0xA0	Operation mode selection
0x06	Configuration	R/W	0x17	Software power down and reset
0x09	Write_Protect	R/W	0x00	Write Protect to avoid missed-writing registers
0x0A	Sleep1	R/W	0x77	Sleep1 configuration
0x0B	Sleep2	R/W	0x10	Sleep2 configuration
0x0D	RES_X	R/W	0x14	CPI resolution setting for X axis
0x0E	RES_Y	R/W	0x14	CPI resolution setting for Y axis
0x12	Delta_XY_Hi	RO	-	High nibble of X-movement and Y-movement for 12-bit 2's complement data format. X-movement = {Delta_XY_Hi[7:4], Delta_X_Lo[7:0]} Y-movement = {Delta_XY_Hi[3:0], Delta_Y_Lo[7:0]}
0x14	Shutter	RO	-	Index of LASER shutter time
0x17	Frame_Avg	RO	-	Average brightness of a frame
0x19	Orientation	R/W	0x04	chip orientation selection

12.2 Register Description

Register Name	Product_ID1							
Bank	0			Address		0x00		
Access	RO			Reset Value		0x31		
Bit	7	6	5	4	3	2	1	0
Field	PID[11:4]							
Description	This value is a unique identification assigned to this model only. The value in this register does not change; it can be used to verify that the serial communications link is functional. PID[11:4] = Product Identifier[11:4].							

Register Name	Product_ID2							
Bank	0			Address	0x01			
Access	RO			Reset Value	0x91			
Bit	7	6	5	4	3	2	1	0
Field	PID[3:0]				VID[3:0]			
Description	This value is a unique identification assigned to this model only. The value in this register does not change; it can be used to verify that the serial communications link is functional. PID[3:0] = Product Identifier[3:0]. VID[3:0] = Product Version[3:0].							

Register Name	Motion_Status							
Bank	0			Address	0x02			
Access	RO			Reset Value	NA			
Bit	7	6	5	4	3	2	1	0
Field	MOTION	Reserved[6:0]						
Description	Typically in the motion detection routine, the host controller will poll the chip for valid motion data by checking the MOTION bit. If the MOTION bit is 1, the motion data in register Delta_X_Lo, Delta_Y_Lo and Delta_XY_Hi is valid and ready to be read. Be sure to check MOTION bit first before reading out register Delta_X_Lo, Delta_Y_Lo and Delta_XY_Hi. DXOVF bit and DYOVF bit show whether if the motion report buffers have overflowed since last read out.							
Field	**Access**	**Reset**	**Description**					
Motion	RO	0	Motion detected since last report 0 : No motion 1 : Motion detected, data in register Delta_X_Lo, Delta_Y_Lo and Delta_XY_Hi is valid and ready to be read out					

Register Name	Delta_X_Lo							
Bank	0			Address	0x03			
Access	RO			Reset Value	NA			
Bit	7	6	5	4	3	2	1	0
Field	Delta_X_7	Delta_X_6	Delta_X_5	Delta_X_4	Delta_X_3	Delta_X_2	Delta_X_1	Delta_X_0
Description	Delta_X_Lo is a 2's complement value in both 8-bit and 12-bit movement data format. In 8-bit format, X-movement = Delta_X_Lo[7:0] In 12-bit format, X-movement = {Delta_XY_Hi[7:4], Delta_X_Lo[7:0]} Register Delta_X_Lo is valid only if register Motion_Status (address 0x02) is read and MOTION bit (bit 7) is 1.							

Register Name	Delta_Y_Lo							
Bank	0			Address		0x04		
Access	RO			Reset Value		NA		
Bit	7	6	5	4	3	2	1	0
Field	Delta_Y_7	Delta_Y_6	Delta_Y_5	Delta_Y_4	Delta_Y_3	Delta_Y_2	Delta_Y_1	Delta_Y_0
Description	Delta_Y_Lo is a 2's complement value in both 8-bit and 12-bit movement data format. In 8-bit format, Y-movement = Delta_Y_Lo[7:0] In 12-bit format, Y-movement = {Delta_XY_Hi[3:0], Delta_Y_Lo[7:0]} Register Delta_Y_Lo is valid only if register Motion_Status (address 0x02) is read and MOTION bit (bit 7) is 1.							

Register Name	Operation_Mode							
Bank	0			Address		0x05		
Access	R/W			Reset Value		0xA0		
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Slp_EnH	Slp2_EnH	Slp1mu_EnH	Slp1mu_EnH	Wakeup
Description	Operation_Mode register allows users to change the chip operation modes. The various combinations of bit4~bit0 are listed below. "0xxxx" = Sleep1 and Sleep2 mode are all disabled "10xxx" = Sleep1 mode is enabled but Sleep2 mode is disable "11xxx" = Sleep1 and Sleep2 mode are all enabled "11100" = Force chip to enter Sleep2 mode "1x010" = Force chip to enter Sleep1 mode "1x001" = Make chip wake up from Sleep mode to Run mode For Slp2mu_EnH / Slp1mu_EnH / Wakeup bit, only one of them can be set to 1 at the same time and the bit which is set will be reset automatically. To force chip always stay at Run mode, please set Slp_EnH=0, Slp2_EnH=0 and Wakeup=1 simultaneously.							

Field	Access	Reset	Description
Slp_EnH	R/W	0	Enable/Disable Sleep mode (including Sleep1 and Sleep2) 0 : Disable (default) 1 : Enable
Slp2_EnH	R/W	0	Enable/Disable Sleep2 mode 0 : Disable (default) 1 : Enable
Slp2mu_EnH	R/W	0	Force to enter Sleep2 mode. Set "1" to enter Sleep2, then it will be reset to "0" automatically
Slp1mu_EnH	R/W	0	Force to enter Sleep1 mode. Set "1" to enter Sleep1, then it will be reset to "0" automatically
Wakeup	R/W	0	Wakeup chip from Sleep mode. Set "1" to wake up, then it will be reset to "0" automatically

Register Name	Configuration							
Bank	0			Address	0x06			
Access	R/W			Reset Value	0x17			
Bit	7	6	5	4	3	2	1	0
Field	RESET	Reserved	Reserved	Reserved	PD_EnH	Reserved	Reserved	Reserved
Description	Configuration register allows users to change the configuration of the chip.							

Field	Access	Reset	Description
RESET	R/W	0	Set “1” to reset all the chip’s internal registers and states, then it will be reset to “0” automatically. Be noticed that after the RESET bit is set on I2C version chip, the host controller should wait at least 1ms and then write this address (0x06) with value 0x17 to ensure the chip has left the reset state.
PD_EnH	R/W	0	Set “1” to enter power down mode for lowest power consumption while retain the chip register settings.

Register Name	Write_Protect							
Bank	0			Address	0x09			
Access	R/W			Reset Value	0x00			
Bit	7	6	5	4	3	2	1	0
Field	Write_Protect[7:0]							
Description	Write Protect register is used to avoid host controller missed-writing the registers beyond address 0x09. 0x00 = Enable (Default), registers beyond address 0x09 are read only 0x5A = Disable, registers beyond address 0x09 can be accessed for read/write							

Register Name	Sleep1							
Bank	0			Address	0x0A			
Access	R/W			Reset Value	0x77			
Bit	7	6	5	4	3	2	1	0
Field	Slp1_Freq[3:0]				Slp1_Etm[3:0]			
Description	Sleep1 register allows users to set the sampling frequency time during Sleep1 mode and the entering time from Run mode to Sleep1 mode.							

Field	Access	Reset	Description
Slp1_Freq	R/W	7	Each step is equivalent to 4ms. Relative to its value 0 ~ 15, the sampling frequency time is 4ms ~ 64ms. Default Slp1_Freq[3:0] =7 (32ms)
Slp1_Etm	R/W	7	Each step is equivalent to 32ms. Relative to its value 0 ~ 15, the entering time is 32ms ~ 512ms. Default Slp1_Etm[3:0] = 7 (256ms)

Register Name	Sleep2							
Bank	0			Address	0x0B			
Access	R/W			Reset Value	0x10			
Bit	7	6	5	4	3	2	1	0
Field	Slp2_Freq[3:0]				Slp2_Etm[3:0]			
Description	Sleep2 register allows users to set the sampling frequency time during Sleep2 mode and the entering time from Run mode to Sleep2 mode.							

Field	Access	Reset	Description
Slp2_Freq	R/W	1	Each step change is equivalent to 64ms. Relative to its value 0 ~ 15, the sampling frequency time is 64ms ~ 1024ms. Default Slp2_Freq[3:0] = 1 (128ms)
Slp2_Etm	R/W	0	Each step is equivalent to 20.48sec. Relative to its value 0 ~ 15, the entering time is 20.48sec ~ 327.68sec. Default Slp2_Etm[3:0] = 0 (20.48sec)

Register Name	RES_X							
Bank	0			Address	0x0D			
Access	R/W			Reset Value	0x14			
Bit	7	6	5	4	3	2	1	0
Field	RES_X[7:0]							
Description	This register is to set the CPI resolution of chip for X-axis (CPI_X). Each step of RES_X is equivalent to 5 counts on flat stainless steel. So, CPI_X = 5 * RES_X. RES_X range: 0 ~ 255 (CPI_X = 0 ~ 1275). Power-up default value of RES_X is 20 (CPI_X = 100). Note: the resolution of a step of RES_X might change across different types of surface, curvature of the surface and distances between chip and surface.							

Register Name	RES_Y							
Bank	0			Address	0x0E			
Access	R/W			Reset Value	0x14			
Bit	7	6	5	4	3	2	1	0
Field	RES_Y[7:0]							
Description	This register is to set the CPI resolution of chip for Y axis (CPI_Y). Each step of RES_Y is equivalent to 5 counts on flat stainless steel. So, CPI_Y = 5 * RES_Y. RES_Y range: 0 ~ 255 (CPI_Y = 0 ~ 1275). Power-up default value of RES_Y is 20 (CPI_Y = 100). Note: the resolution of a step of RES_Y might change across different types of surface, curvature of the surface and distances between chip and surface.							

Register Name	Delta_XY_Hi						
Bank	0			Address	0x12		
Access	RO			Reset Value	NA		
Bit	7	6	5	4	3	2	1	0
Field	$Delta\_X_{11}$	$Delta\_X_{10}$	$Delta\_X_9$	$Delta\_X_8$	$Delta\_Y_{11}$	$Delta\_Y_{10}$	$Delta\_Y_9$	$Delta\_Y_8$
Description	Delta_XY_Hi is the high nibble of both X-movement and Y-movement for 12-bit 2's complement data format. X-movement = {Delta_XY_Hi[7:4], Delta_X_Lo[7:0]} Y-movement = {Delta_XY_Hi[3:0], Delta_Y_Lo[7:0]} Register Delta_XY_Hi is valid only if register Motion_Status (address 0x02) is read and MOTION bit (bit 7) is 1.							

Register Name	Shutter							
Bank	0			Address	0x14			
Access	RO			Reset Value	NA			
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Shutter[5:0]					
Description	Shutter register is an index of LASER shutter time. It is automatically controlled by the chip's internal auto-exposure algorithm. When the chip is tracking on a good reflection surface, the Shutter is small. When the chip is tracking on a poor reflection surface, the Shutter is large. Value ranges from 0 to 46.							

Register Name	Frame_Avg							
Bank	0			Address	0x17			
Access	RO			Reset Value	NA			
Bit	7	6	5	4	3	2	1	0
Field	Frame_Avg[7:0]							
Description	Frame_Avg register represents the average brightness of all pixels within a frame (324 pixels). This value ranges from 0(darkest) to 255(brightest).							

<table>
<tr><th>Register Name</th><th colspan="8">Orientation</th></tr>
<tr><td>Bank</td><td colspan="3">0</td><td colspan="2">Address</td><td colspan="3">0x19</td></tr>
<tr><td>Access</td><td colspan="3">R/W</td><td colspan="2">Reset Value</td><td colspan="3">0x04</td></tr>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Field</td><td>Reserved</td><td>Reserved</td><td>XY_SW</td><td>Y_INV</td><td>X_INV</td><td>XY12bit_Enh</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Description</td><td colspan="8">To change the X/Y direction to accommodate to different chip orientations.</td></tr>
</table>

Field	Access	Reset	Description
XY_SW	R/W	0	To swap the X and Y direction.
Y_INV	R/W	0	To invert the Y direction.
X_INV	R/W	0	To invert the X direction.
XY12bit_Enh	R/W	1	To select 8-bit or 12-bit motion data length for X-movement and Y-movement. 0 : 8-bit mode 1 : 12-bit mode (default)

Document Revision History

Revision Number	Date	Description
0.1	02 May 2016	Preliminary release
0.2	15 May 2016	1. Modified the operation current 2. Added power-up sequence
0.3	03 June 2016	1. Added SPI mode 3 constraint on Chapter 8.0 2. Modified the spec of $t_{PREP-RD}$ from 10us to 250ns
0.4	15 June 2016	1. Rephrased the description in power-up sequence requirements. 2. Added the parameter spec for "Distance from chip Top to Tracking Surface" in Table. 3 3. Rephrased the description in Methods to Read the Motion Data
0.5	22 Aug. 2016	1. Modify the flowchart of Figure 34. Read Motion Data with Interrupt Mode
0.6	25 Aug. 2016	1. Corrected some typos. 2. Modify the flowchart of Figure 34. Read Motion Data with Interrupt Mode
0.7	10 Oct. 2016	1. Modified "Max .Tracking Speed" in page 1 from 10ips to 30ips 2. Modified "Distance from chip top to tracking surface" in page 1 from 2 ~ 10mm to 1 ~ 30mm 3. Add speed and counts/rev. spec. in page 1 for 1.0mm diameter STS shaft 4. Modify the flowchart of Figure 34. Read Motion Data with Interrupt Mode 5. Modified Motion bit to MOTION bit (in capital) 6. Modified the max I2C clock speed from 1MHz to 400KHz in Table 5 7. Change I2C $t_{SU.DAT}$ (Data setup time) in Table 5 from 100ns to 250ns 8. Rephrased the description in Section 10.3 Software Reset 9. Added 9th pin (PixArt testing pin) in Table 1 10. Added 9th pin in Figure 9
0.8	04 Nov. 2016	1. Rephrased the power up sequence in Section 4.0
1.0	06 Jan. 2017	1. Added the dimension of the hole of pin 9 in Figure 9. 2. Corrected the typo of x097 to 0x97 in Section 10.3. 3. Corrected the reset value of Slp2_Freq and Slp2_Etm to 1 and 0 respectively. 4. Removed Laser Drive Current spec. in Table 3 5. Added CPI vs Speed @Different distance in Figure 8